Preparatory Test

Dept:EC	Sem / Div:III A&B	Sub:Digital System Design	S Code:18EC34
Date:25-02-2021	Time: 10:0-1:00 pm	Max Marks: 100	Elective:N
Note: Answer any 5 full questions, choosing one full question from each Module.			

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QN		Questions	Marks	RBT	COs
		Module 1			
1	a	Design a combinational circuit to output the 2's complement of a 4-bit binary number	7	L3	CO1
	b	Identify Prime Implicants and Essential Prime Implicants of the following Boolean function: f(a,b,c,d)=Σ(0, 1, 4, 6, 7, 9, 15)+Σd(3, 5, 11, 13). Draw the diagram using NOR gates.	7	L2	CO1
	c	Expand the following into canonical form I) f1=a+bc+ac'd into minterms II) f2=a(b+c)(a+c+d) into maxterms	6	L2	CO1
		OR			
2	a	Find minimal sum of the following boolean function using Quine McCluskey Method (a,b,c,d)= Σm(2,3,4,5,13,15) + d(8,9, 10,11)	7	L2	CO1
	b	Obtain minimal expression using k-map for the following incompletely specified function: F(a,b,c,d)= Σm(0,1,4,6,7,9,15)+ d(3,5,11,13) and draw the circuit diagram using NAND gates	7	L2	CO1
	c	Explain Prime Implicants, Essential Prime Implicant, Canonical SOP, Canonical POS and Minterm.	6	L2	CO1
		Module 2			
3	a	Design 4 to 16 decoder using 3 to 8 decoder(74138) and Realize the function using 74138: a) P=f(w,x,y,z)=Σ(1,4,8,13) b) Q=f(a,b,c,d)=Σ(2,7,13,15)	7	L3	CO2
	b	Define encoder. Design 4-bit priority encoder with validity output which gives MSB the highest priority and LSB the least Priority.	7	L3	CO2
	c	Explain 4-bit carry look ahead adder with necessary diagram and relevant expression	6	L2	CO2
		OR			
4	a	Implement the function f(a,b,c,d)= Σm(0,1,3,4,8,9,15) using: a) 4:1 mux with a,c as select lines b) 8:1 mux with a,b,d as select lines	6	L3	CO2
	b	Define magnitude comparator. Design a combinational circuit that compares two 2-bit binary number and provides 3 outputs	8	L3	CO2
	c	Explain the structure of PLA with an example.	6	L2	CO2
		Module 3			
5	a	Explain Master Slave JK flip-flop with the help of circuit diagram and waveforms	8	L2	CO3
	b	Explain clocked SR-FF using NAND gates with necessary truth table and waveform.	6	L2	CO3
	c	Explain universal shift register.	6	L2	CO3
		OR			

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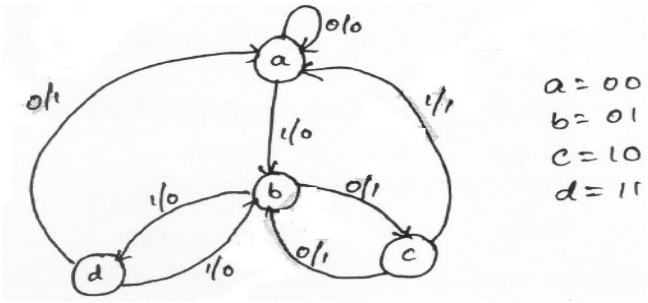
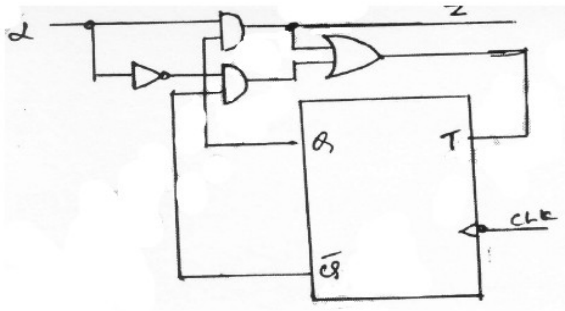
6	a	Explain the concept of Twisted Ring counter with neat circuit diagram	7	L2	CO3
	b	Explain 4-bit synchronous binary up counter.	7	L2	CO3
	c	Find characteristic equation for SR flip-flop and JK flipflop with the help of function table.	6	L2	CO3
		Module 4			
7	a	Design mod-6 counter using D-flipflop. The sequence is 000, 001, 011, 100, 101, 111,..000.	10	L3	CO3
	b	Design a clocked sequential circuit which operates according to the state diagram shown in the figure below. Implement the circuit using negative edge triggered JK fliflop 	10	L3	CO3
		OR			
8	a	Analyze the following sequential circuit. Construct transition table, state table and state diagram. 	10	L3	CO3
	b	Realize synchronous decade counter using T-FF and draw the diagram	10	L3	CO3
		Module 5			
9	a	Construct a Mealy state diagram that will detect input secuence 1011, when input pattern is detected Z is asserted high.	10	L3	CO4
	b	Explain with block diagram Serial Adder with accumulator	10	L2	CO3
		OR			
10	a	Design a iterative circuit which compares two n-bit binary numbers and determines if they are equal or which one is larger if they are not equal.	10	L3	CO4
	b	Construct the state diagram for Excess-3 to BCD code converter.	10	L3	CO4